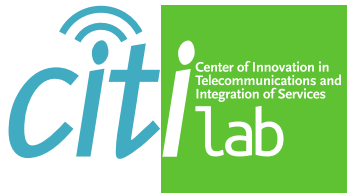
FPGA-based Implementation of Multiple PHY Layers of IEEE 802.15.4 Targeting SDR Platform

Abdelbassat MASSOURI & Tanguy RISSET

SDR-WinnComm 11 March 2014 ∼ Schaumburg, Illinois



OUTLINE

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MOTIVATION

Limited Cognitive Radio Testbeds

- Cognitive radio networks is a major research challenge (NSF 2009).
- Develop a set of cognitive networking testbeds in order to enhance spectrum reuse and sharing.
- Numerous WSN testbeds & few large-scale Cognitive radio testbeds.
- ORBIT, CORNET... : Deployed in conventional environment (interference) & CR nodes are USRPs (Real-time & BW limitation)

SDR Technology Affordability

- SDR technology has been accessible at reasonable price only recently
- USRPs (Ettus/NI), PicoSDR/ZeptoSDR (Nutaq), miniBEE (BEEcube)...

Lack of Open Source HDL IPs

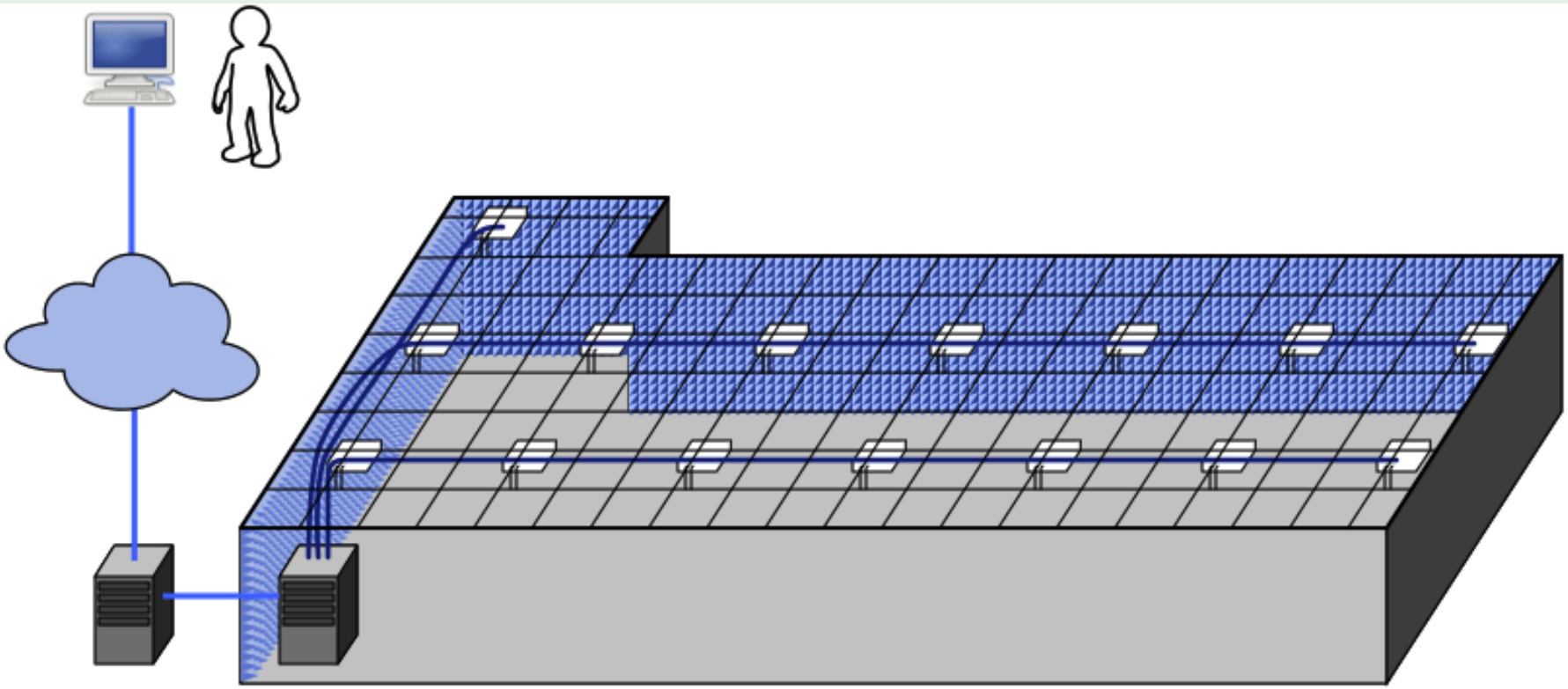
- Open source software vs open source hardware
- OpenCores provides mainly processors and their peripherals

OUTLINE

CorteXlab : A New Facility for Testing SDR & Cognitive Radio Networks

New Cognitive Radio Testbed

- FIT : Future Internet of Things (French funding)
- $167m^2$ EM shielded room & completely faradized ($80dB$ of attenuation in the band $[0.5 - 5]GHz$)
- x40 SDR Nodes & x42 WSN Nodes (ZigBee)
- Free Remote Access & Experiment Control Middleware



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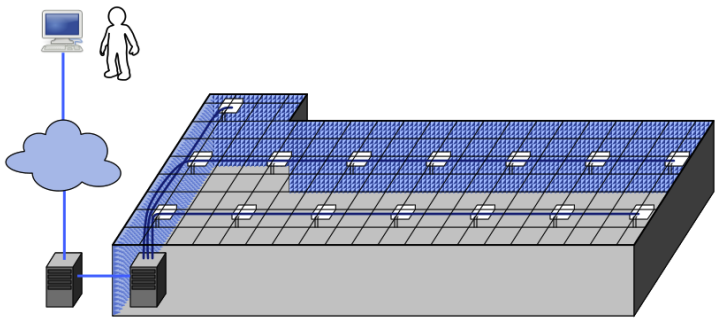

SDR Technology

- x22 USRPs : SISO, [0.4 – 4]GHz, BW=20MHz
- x12 2x2 & x6 4x4 PicoSDRs : Virtex-6 FPGA, MIMO, [0.3 – 3.8]GHz, BW=28MHz

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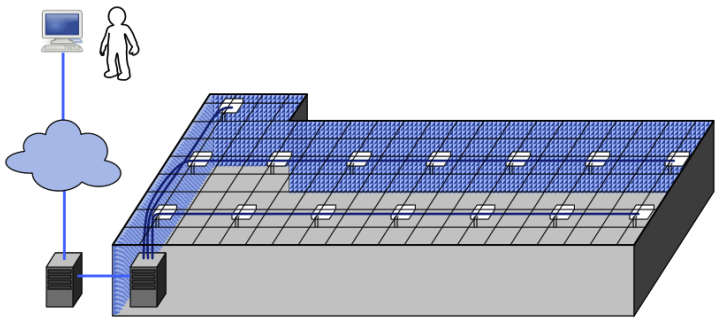

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Open Source HDL IPs (VHDL)

- Open source hardware (HDL) toolbox
- FPGA-based Design For GNU radio users
- FPGA-based IEEE 802.15.4 baseband IPs
- FPGA-based MIMO-OFDM baseband IPs

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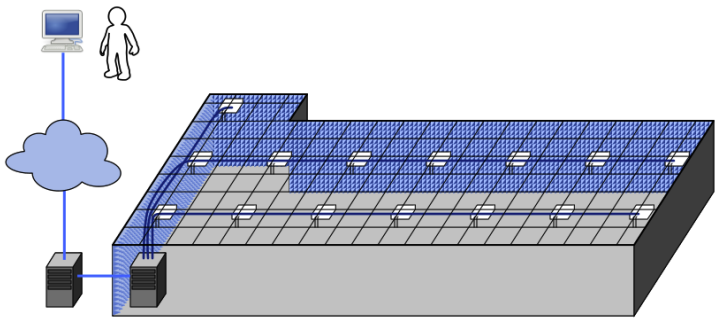

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FPGA-based IEEE 802.15.4 baseband IPs

- FPGA-based implementation of IEEE 802.15.4 baseband PHY layers on PicoSDR platform

OUTLINE

IEEE 802.15.4 : PHY Layers & Baseband Specifications

PHY Options

- Option 1
- Option 2
- Option 3

PHY (MHz)	Frequency Band (MHz)	Spreading Parameters		Data Parameters		
		Chip rate (kchips/s)	Modulation	Bit rate (kb/s)	Symbol Rate (ksymbol/s)	Symbols
868/915	868-868.6	300	BPSK	20	20	Binary
	902-928	600	BPSK	40	40	Binary
2450	2400-2483.5	2000	O-QPSK	250	62.5	16-ary Orthogonal

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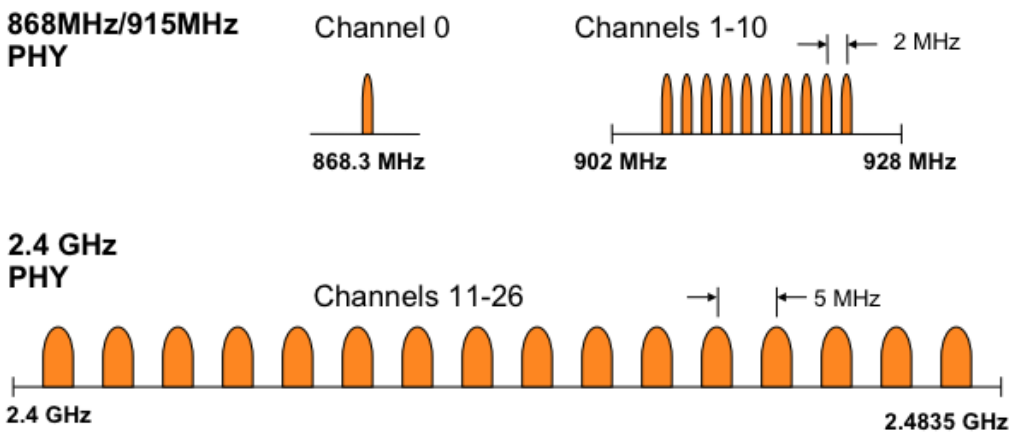
PHY Options 1 & 2 vs PHY Option 3

- Options 1 & 2 DS-SS : 2 PNS (15 Bits)
- Options 3 DS-SS : 16 PNS (32 Bits)
- Options 1 & 2 Shaping Filter : Raised Cosine Filter
- Options 3 Shaping Filter : Half Sine Filter



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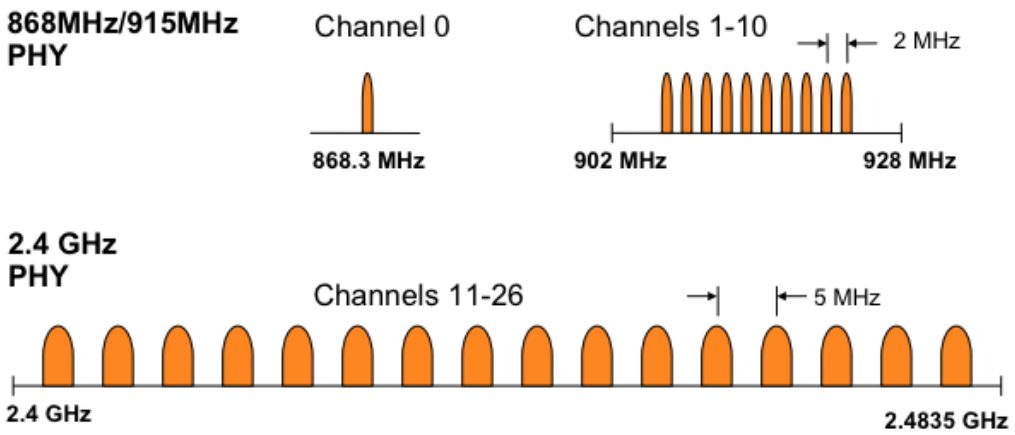
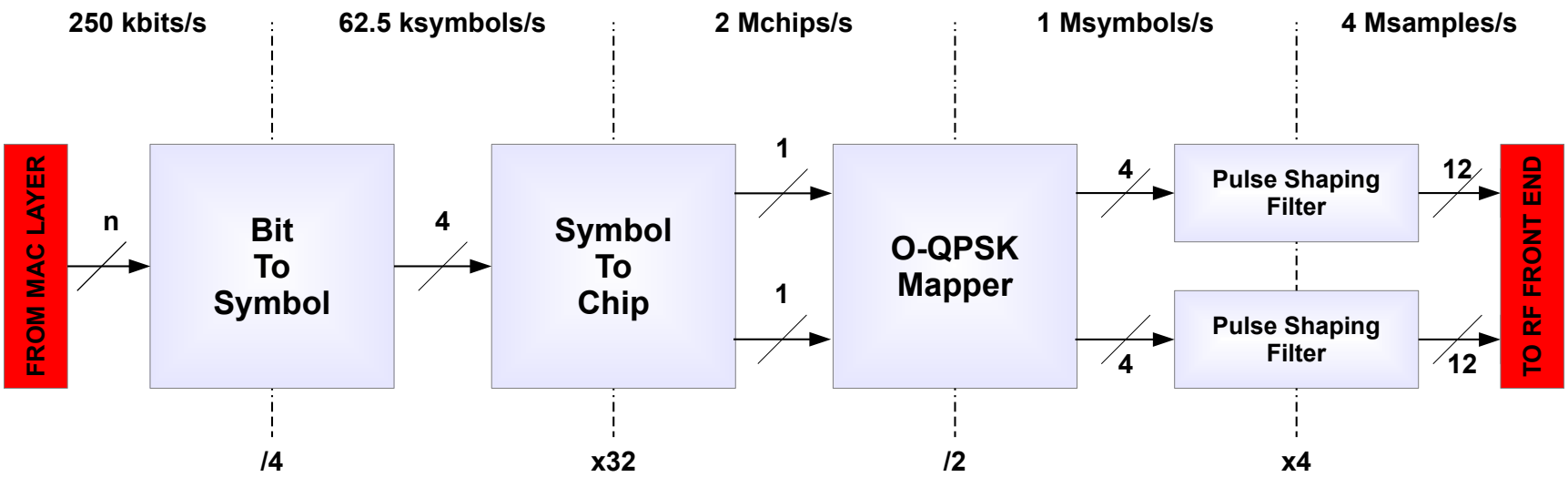


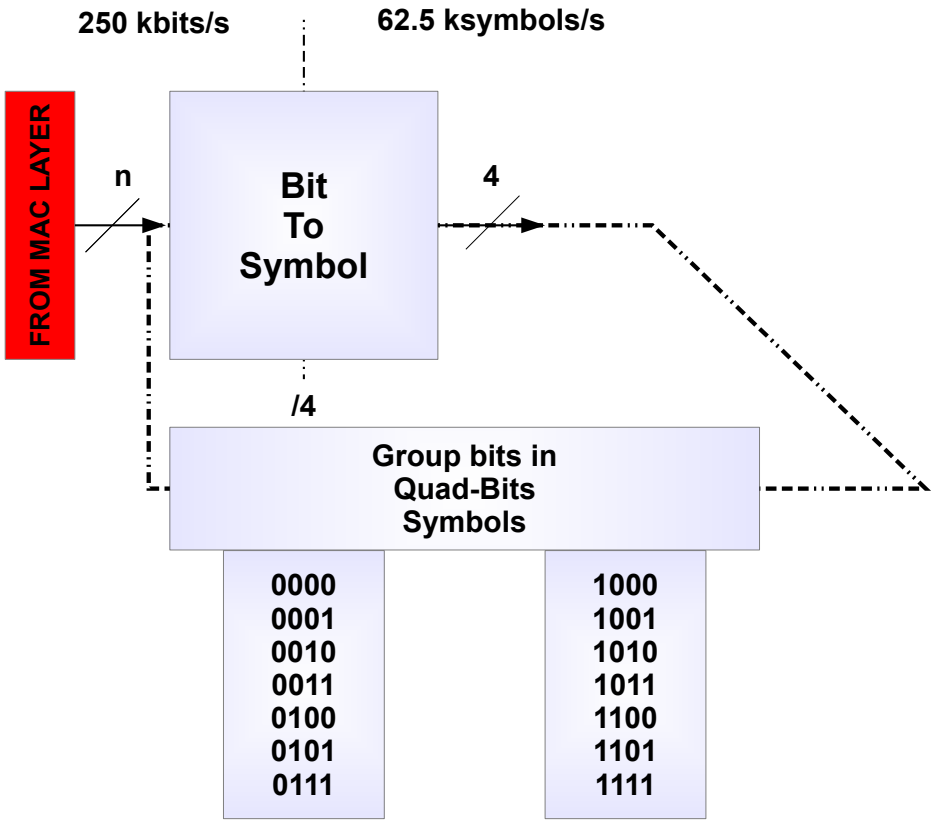
IEEE 802.15.4 PHY Layer : Option 3 TX/RX Architectures

- TX Architecture
- RX Architecture

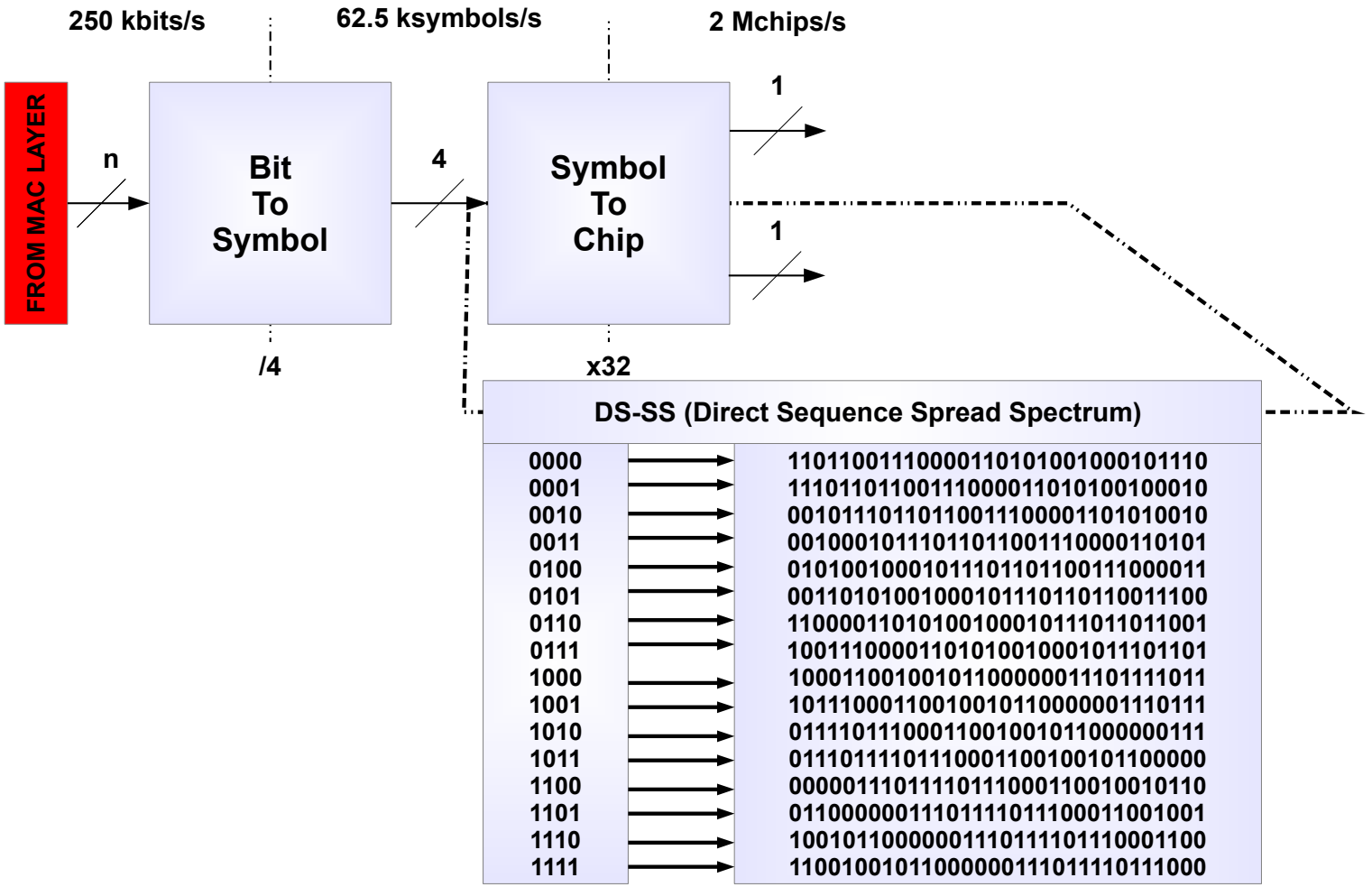
IEEE 802.15.4 PHY Layer Option 3 : TX BB Architecture



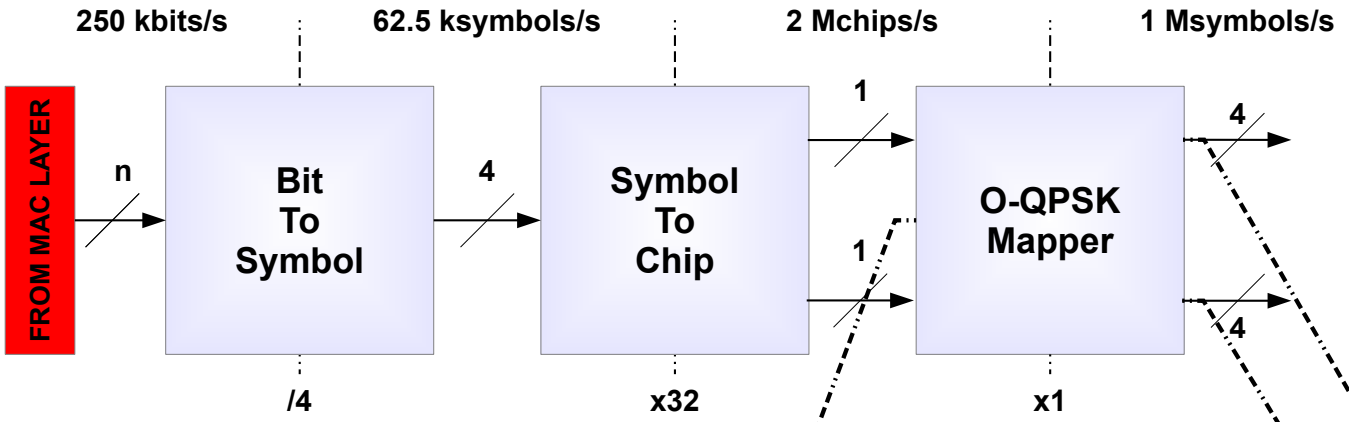
IEEE 802.15.4 TX Option 3 : Bit To Symbol



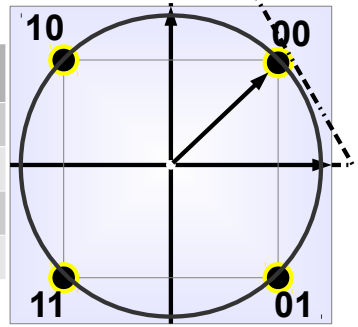
IEEE 802.15.4 TX Option 3 : DS-SS (Direct Sequence Spread Spectrum)



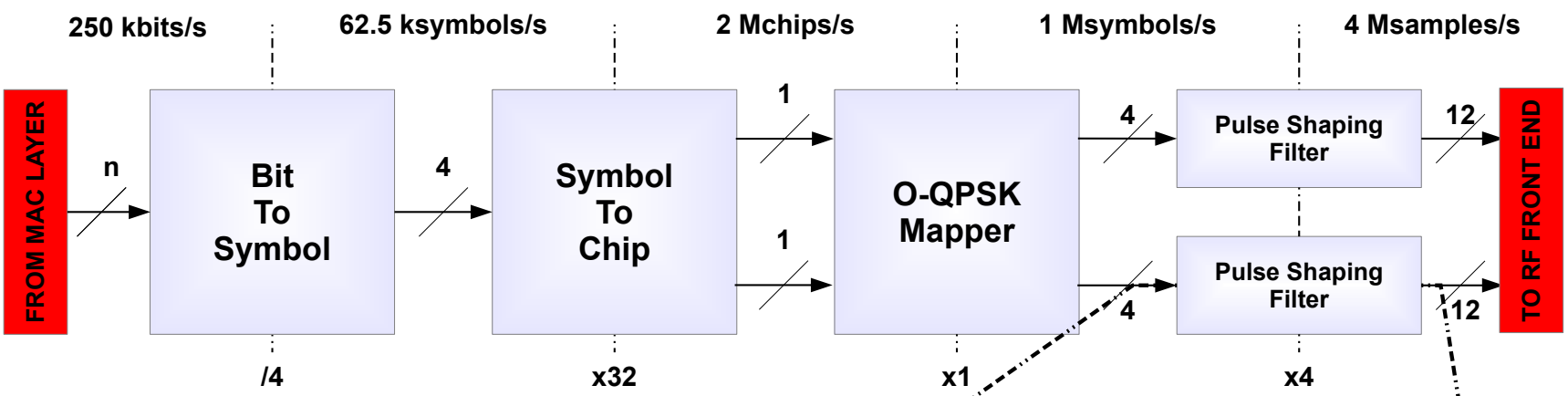
IEEE 802.15.4 TX Option 3 : QPSK Mapping

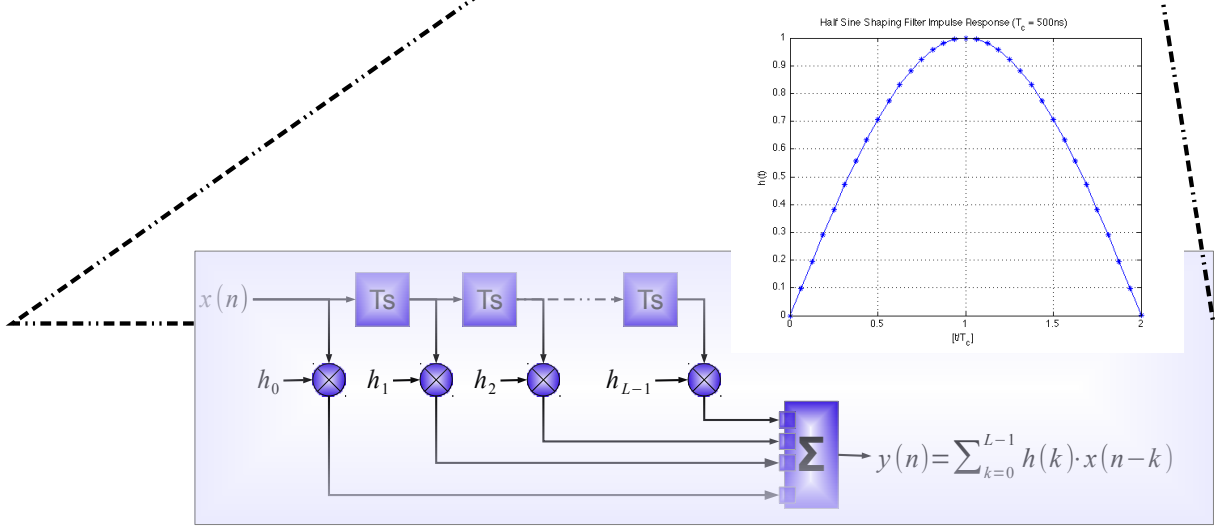


$b_0 b_1$	θ_k	$s_k^I = \sqrt{(2)}\cos(\theta_k)$	$s_k^Q = \sqrt{(2)}\cos(\theta_k)$
00	$\pi/4$	$+\sqrt{E/2}$	$+\sqrt{E/2}$
10	$3\pi/4$	$-\sqrt{E/2}$	$+\sqrt{E/2}$
11	$5\pi/4$	$-\sqrt{E/2}$	$-\sqrt{E/2}$
01	$7\pi/4$	$+\sqrt{E/2}$	$-\sqrt{E/2}$

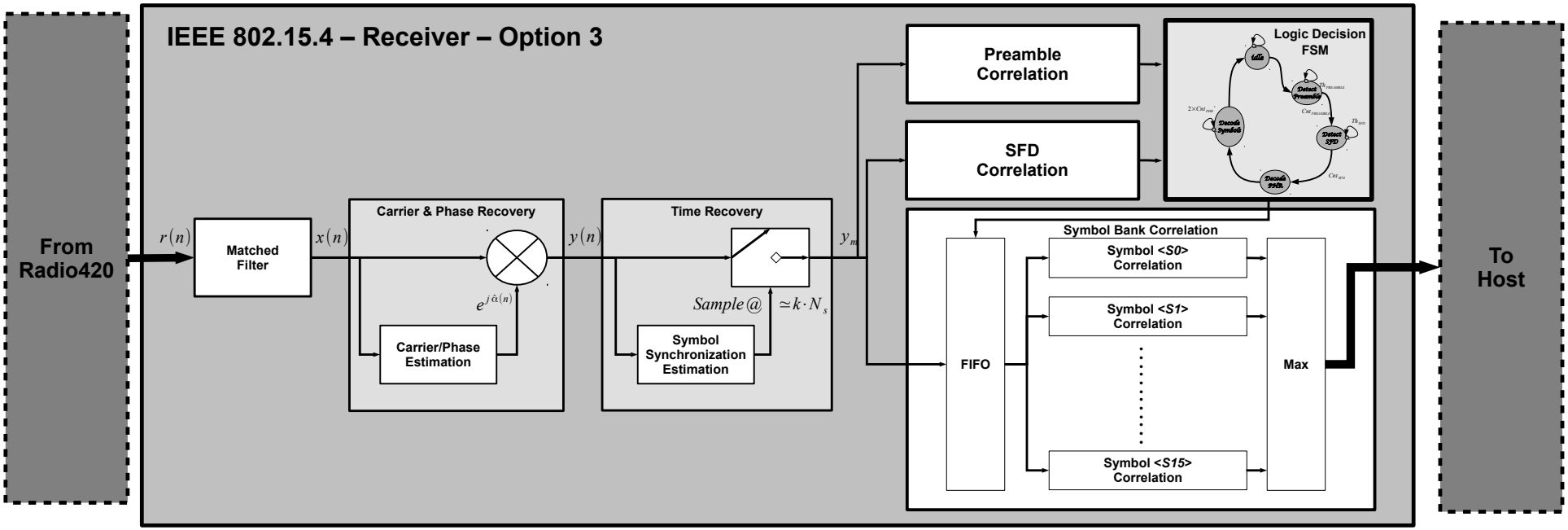


IEEE 802.15.4 TX Option 3 : Shaping Filter





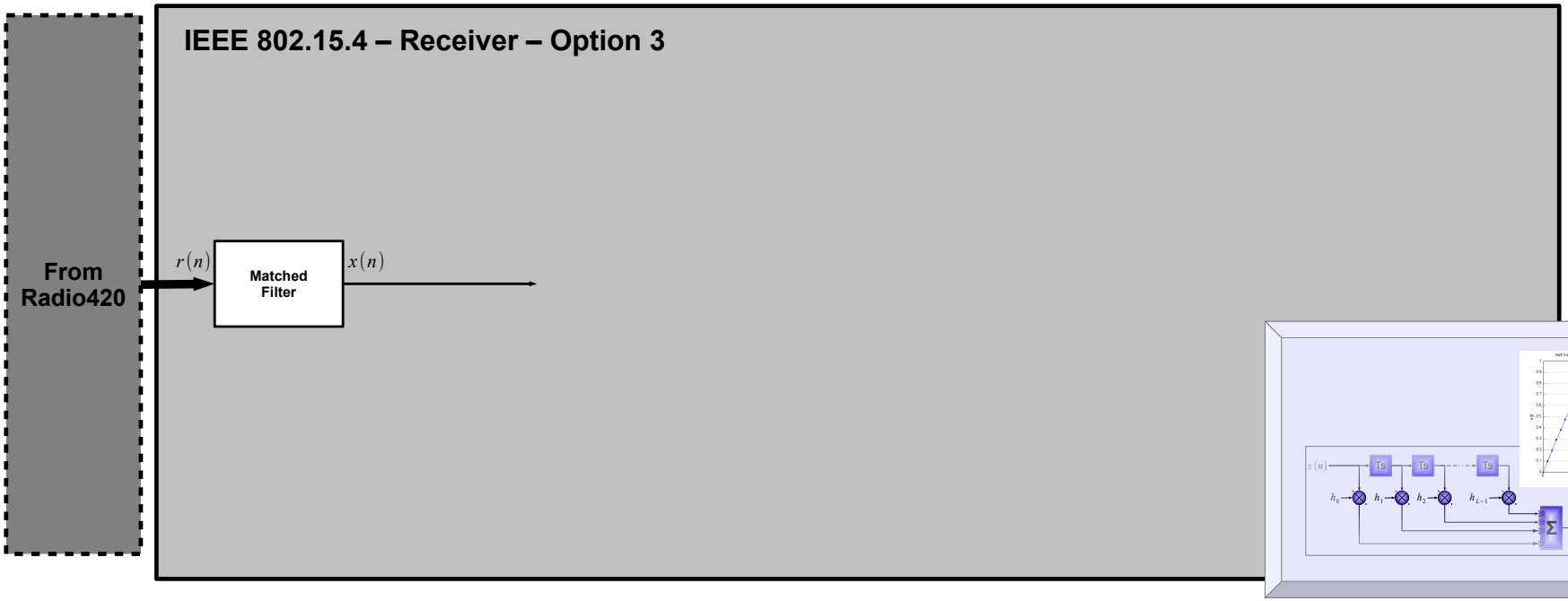
IEEE 802.15.4 PHY Layer Option 3 : RX BB Architecture



Option 3 Receiver vs Option 1 & 2 Receiver

- They share most of the blocs except the matching filter coefficients and Bank Symbol Correlator
- Option 3 receiver has 16 symbols correlators while Option 1 & 2 receiver has only one symbol correlator

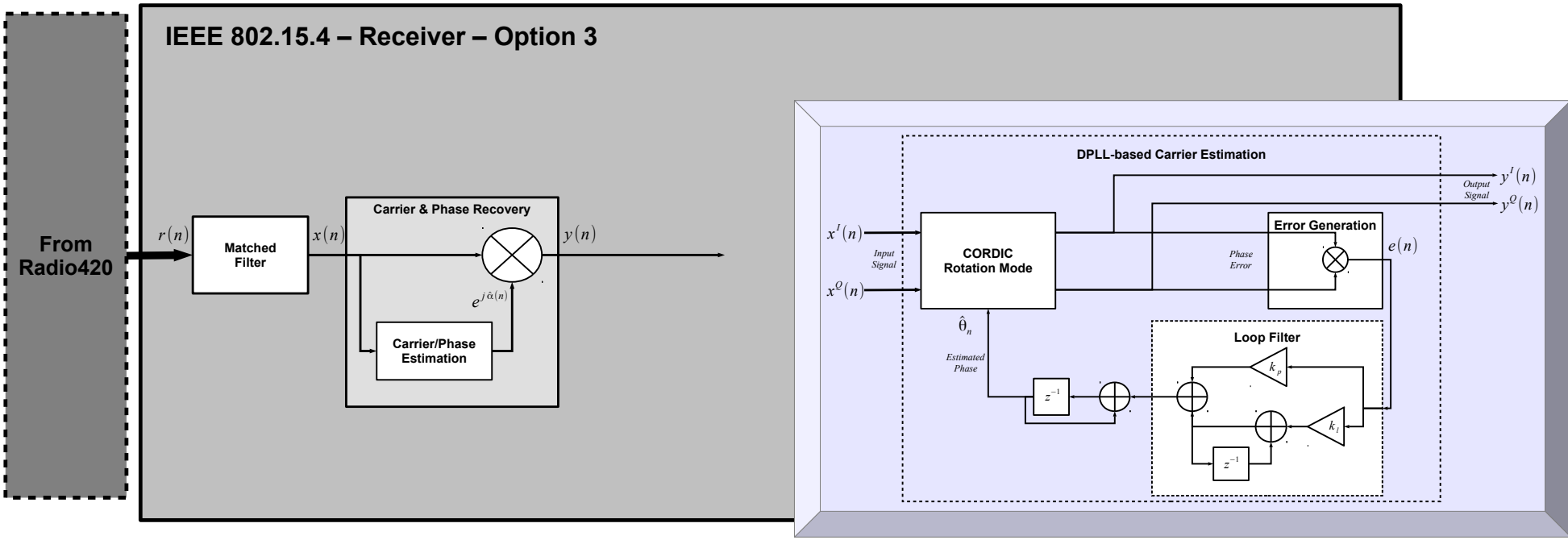
IEEE 802.15.4 RX Option 3 : Matching Filter



Matching Filter

- Option 3 receiver : Half Sine Filter
- Option 1 & 2 receiver : Raised Cosine Filter

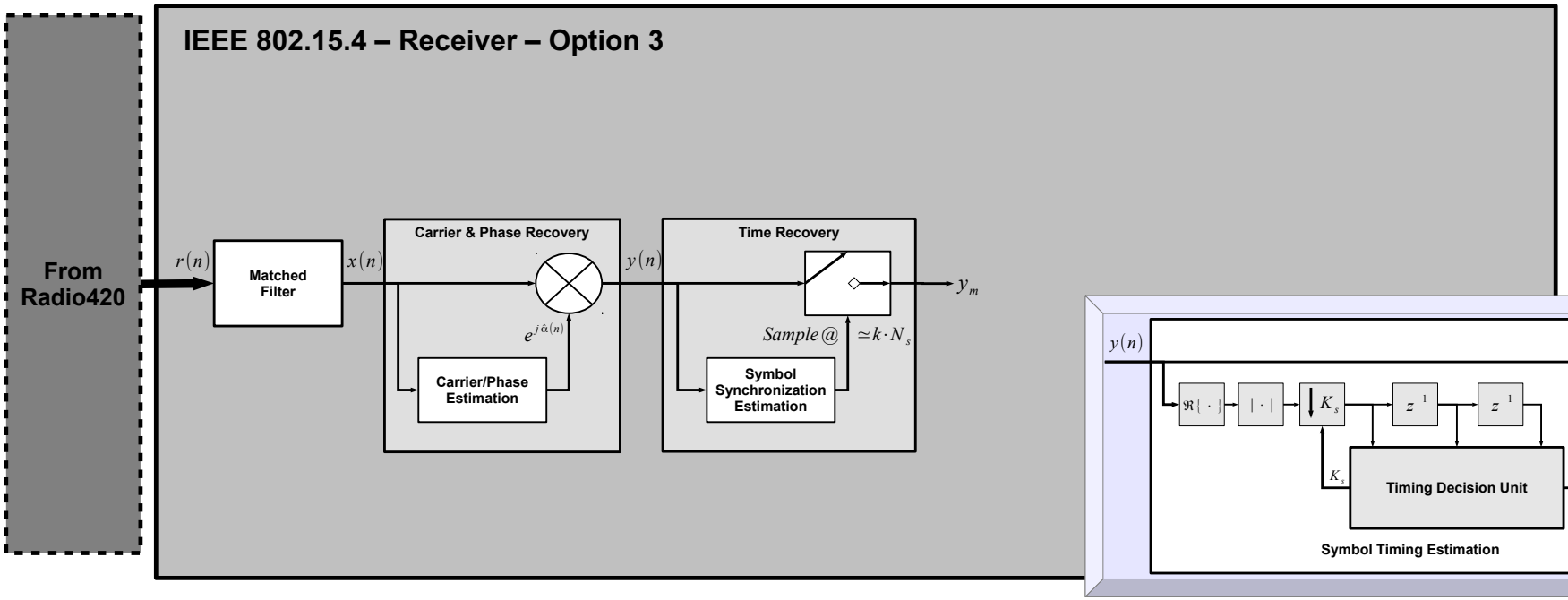
IEEE 802.15.4 RX Option 3 : Phase & Frequency Recovery



Phase & Frequency Recovery

- DPLL : Digital Phase Locked Loop
- Phase Detector, Loop Filter, DCO
- CORDIC Algorithm in rotation mode

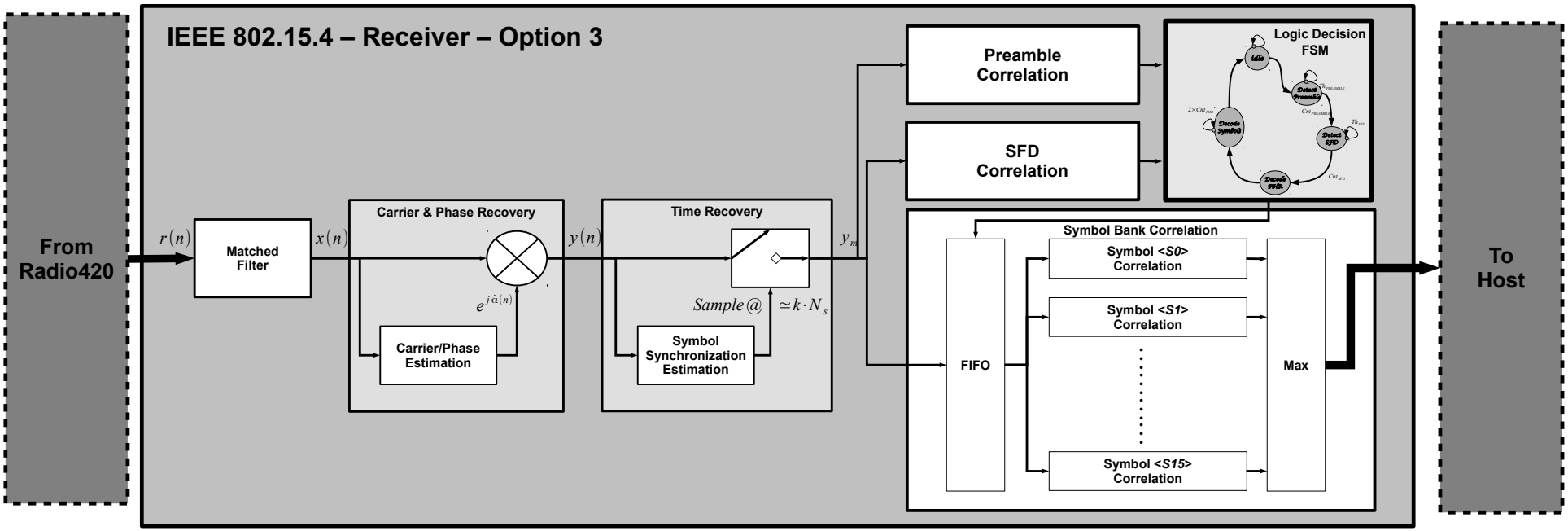
IEEE 802.15.4 RX Option 3 : Symbol Timing Recovery



Symbol Timing Recovery

- Early Late Gate Algorithm
- Timing Decision Control Unit

IEEE 802.15.4 RX Option 3 : Symbol Decoder



Symbol Decoder

- Preamble Correlator
- SFD (Start of Frame Delimiter) Correlator
- Bank of Symbol Correlators
- FSM (Finite State Machine) to control the state of correlators
- The decoded symbol is the binary code of the index of the symbol correlator having the maximum correlation value [0 – 15].

IP Core	Logic Utilization	Used	Available	Utilization
Transmitter Option 1 & 2	Slice Registers	150	393600	0.038%
	Slice LUTs	140	196800	0.071%
	Occupied Slices	72	49200	0.146%
Transmitter Option 3	Slice Registers	269	393600	0.068%
	Slice LUTs	230	196800	0.117%
	Occupied Slices	115	49200	0.234%
Receiver Option 1& 2	Slice Registers	1499	393600	0.381%
	Slice LUTs	1709	196800	0.868%
	Occupied Slices	652	49200	1.325%
	DSP48s	23	1344	1.711%
Receiver Option 3	Slice Registers	1879	393600	0.477%
	Slice LUTs	1758	196800	0.893%
	Occupied Slices	697	49200	1.417%
	DSP48s	57	1344	4.241%
IEEE 802.15.4 TX/RX total	Slice Registers	3797	393600	0.964%
	Slice LUTs	3837	196800	1.949%
	Occupied Slices	1536	49200	3.122%
	DSP48s	80	1344	5.958%

Virtex-6 XC6SX315T FPGA Target : Ressource utilization

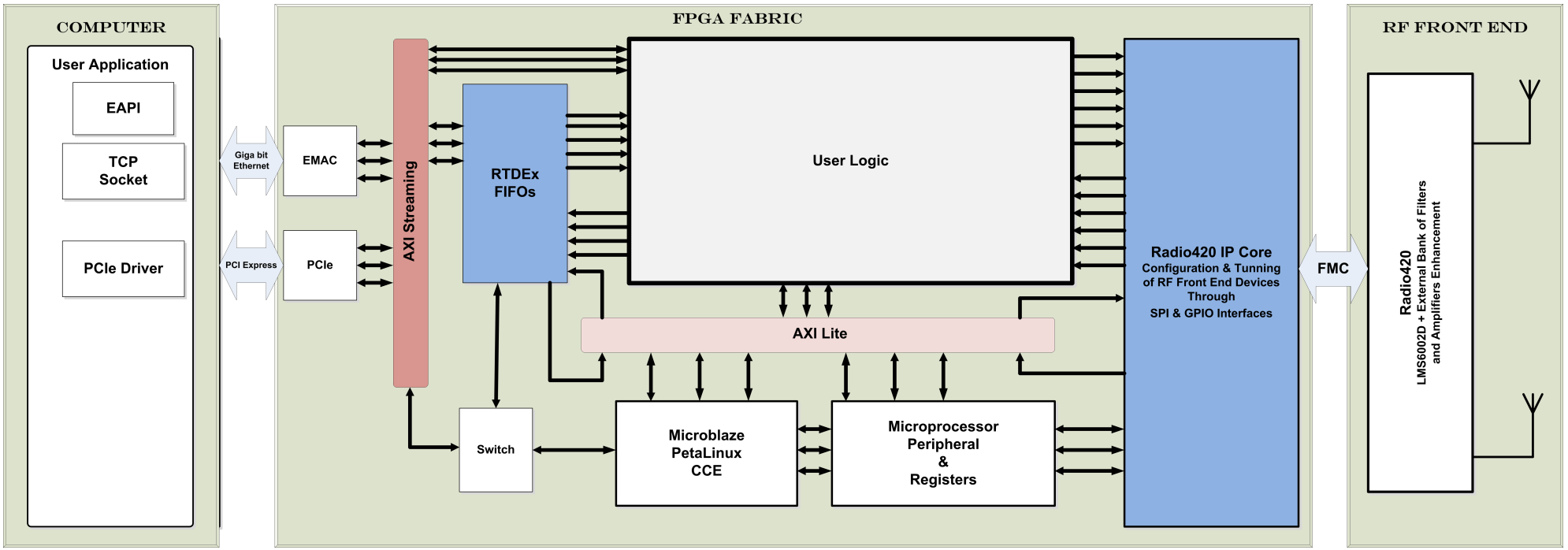
- Transmitters & Receivers of both option 1 & 2 and option 3 resource utilization are $< 5\%$.
- Multiple PHY Layers FPGA-based implementation on the PicoSDR Platform

OUTLINE

PicoSDR : HW & SW Framework & BSDK Design Flow

FPGA & RF Front End

- Perseus 6011 : Virtex-6 VC6SX315T : Logic Slices, DSP48, BRAM, EMAC, PCIe...
- Radio420 : LMS6002D, Analog Bank Filter, External PA & LNA



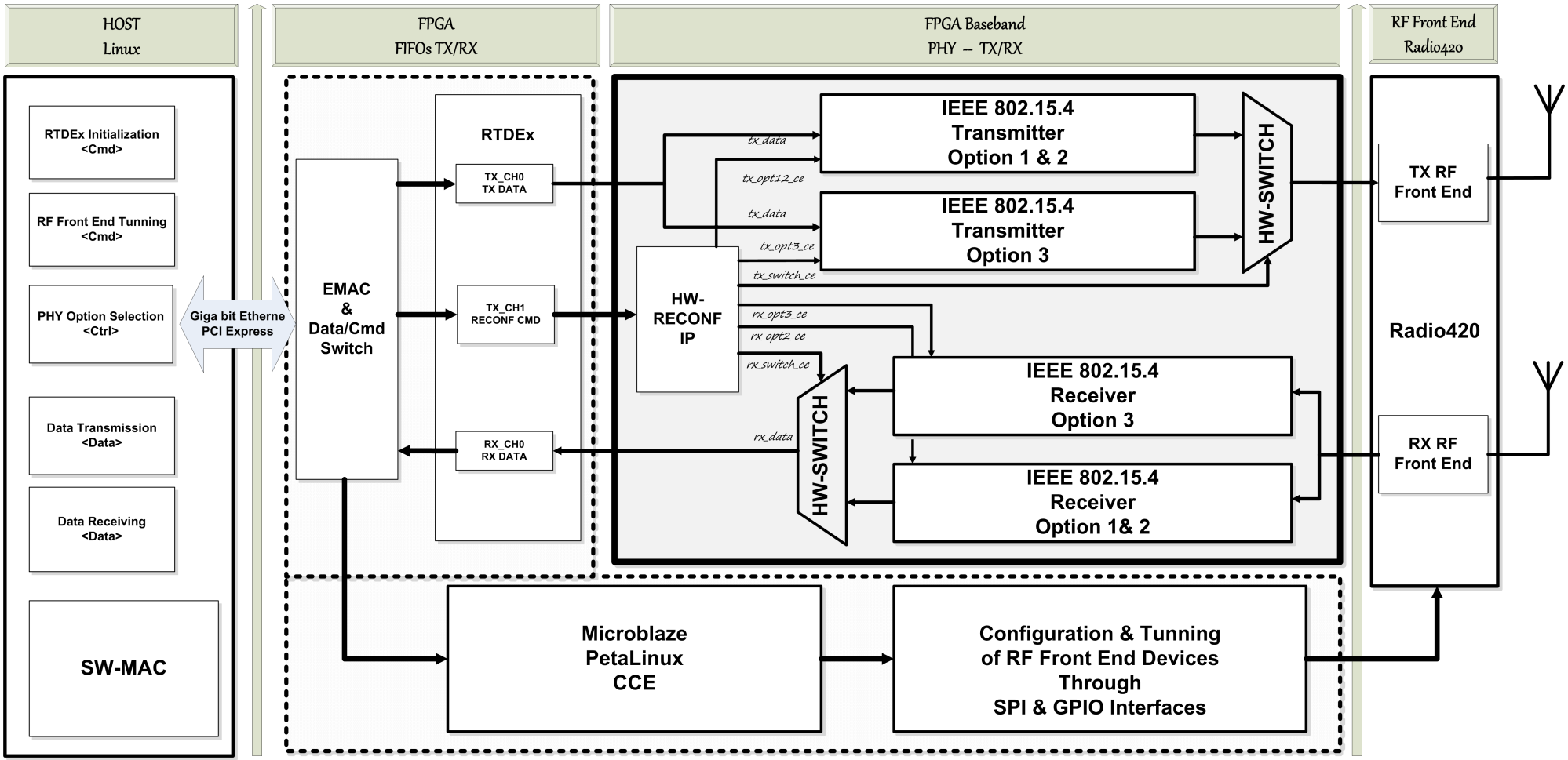
FPGA Fabric

- RTDEx : x8 TX & x8 RX FIFOs
- User Logic Space : Multiple Transmitter / Multiple Receiver & Control FSM

IEEE 802.15.4 : Multiple PHY Layers Implementation on PicoSDR Platform

BSDK Design Flow

- Host (Linux OS) running C program (Soft MAC, RF Front End tuning...)
- User Logic implementing Multiple Transmitters & Receivers, Control FSM, Switches...



OUTLINE

FUTURE WORK

IEEE 802.15.4

- HW/SW Co-design of MAC Layer
- Test & Validation of CorteXlab IEEE 802.15.4 Design with commercial Zigbee Wireless Sensor Node (ATMEL AT86RF231 2.4GHz Transceiver)

MIMO-OFDM

- Multiple Carrier (OFDM) FPGA-based Design
- MIMO-OFDM FPGA-based Design

Source Code

- Open Source HDL Code (VHDL)
- CeCILL Licence / CorteXlab : http ://www.cortexlab.fr

THANK YOU

FIT/CorteXlab : Cognitive Radio Tesbed

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